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UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,288	04/20/2004	Kazuo Sakamoto	XA-10084	2625

			EXAMINER
181	7590	06/26/2006	RAHMAN, FAHMIDA

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ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 06/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/827,288	SAKAMOTO ET AL.
	Examiner	Art Unit
	Fahmida Rahman	2116

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2004*.

2a)☐ This action is **FINAL**.　　2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

　　4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

　　Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　　a)☐ All　b)☐ Some *　c)☐ None of:

　　　1.☐ Certified copies of the priority documents have been received.

　　　2.☐ Certified copies of the priority documents have been received in Application No. _____.

　　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

　　* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date *4/20/2004*.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____ .

DETAILED ACTION

1.   Claims 1-11 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 4/20/2004 is in compliance

with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is

being considered by the examiner.

Priority

2.   Acknowledgment is made of applicant's claim for foreign priority under 35

U.S.C. 119(a)-(d). The certified copy filed on 8/4/2004 has been received.

Should applicant desire to obtain the benefit of foreign priority under 35 U.S.C. 119(a)-

(d) prior to declaration of an interference, a translation of the foreign application should

be submitted under 37 CFR 1.55 in reply to this action.

Drawings

Figure 7 and Figure 8 should be designated by a legend such as --Prior Art-- because

only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in

compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid

abandonment of the application. The replacement sheet(s) should be labeled

"Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct

any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 5 and 10 is objected to because of the following informalities:

"said storage device" in line 3 of claim 5 should be "a storage device" as it is recited for the first time.

"resistor" in line 3 of claim 10 is not appropriate as resistor cannot store any value. This should be changed to register.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "a clock signal" in line 16. It is unclear whether it is

intended to be the same or different from "a clock signal" mentioned in line 4. It is

necessary to establish a relationship between two "a clock signal" mentioned in line 4

and line 16.

Claim 11 recites the limitation "a clock signal" in line 5. It is unclear whether it is

intended to be the same or different from "a clock signal" mentioned in lines 4 and 16 of

claim 1. It is necessary to establish a relationship among all recitations of "a clock

signal".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4, 5, 6, 9, 10, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable

over AAPA, in view of Schaefer (US Patent Application Publication 2005/0243635).

For claim 1, AAPA teaches the following limitations:

A data processing device formed as a semiconductor integrated circuit

("microcomputer" in lines 19-23 of page 2), which is coupled to an external device

("memory cards" in lines 19-23 of page 2) for performing data transmission and

reception in synchronization with a clock signal (lines 19-23 of page 2), said data

processing device comprising:

a central processing unit ("microcomputer" must have a CPU); an interface unit (200)

for data transmission and reception to and from the external device (Fig 7), wherein said

interface unit includes:

an external terminal for outputting said clock signal (241);

an output driver (252) for driving said external terminal to output said clock signal (Fig

7); an equivalent load circuit (G3) to generate a clock signal (CLK') for latching data

inputted from said external device (242-254-255 of Fig 7).

The AAPA does not teach the following limitations:

an equivalent load circuit capable of imparting, to the clock signal extracted from an

arbitrary position in a stage previous to output driver in a clock signal path, delay

equivalent to delay resulting from an external load coupled to external terminal in-order

to generate a clock signal for latching data inputted from said external device.

Schaefer teaches the following limitations:

an equivalent load circuit (210) capable of imparting, to the clock signal (202) extracted

from an arbitrary position in a stage previous (CLKD) to output driver (combination of

212a-i and 213a-i are DQ buffers, which are output drivers) in a clock signal path (CLKD

is on the clock signal path) , delay equivalent to delay resulting from an external load

coupled to external terminal (The output driver or buffers are connected to external load.

The output buffer must consider the loading condition, which includes the delay associated with the load. Thus, delay B must incorporate the delay of load. A supporting statement can be found in lines 6-15 of [0005] of page 1, which mention that clock can be offset with delay compensation circuit for variations such as loading conditions. Thus, the loading conditions are communicated to the delay model 210)

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of AAPA and Schaefer. One ordinary skill in the art would have been motivated to have an equivalent circuit with variable load delay, since that places the data valid window with greater precision (line 15 of [0005] of page 1).

For claim 4, AAPA teaches the following limitations:

A data processing device formed as a semiconductor integrated circuit ("microcomputer" in lines 19-23 of page 2), which is coupled to a memory device ("memory cards" in lines 19-23 of page 2) for performing data transmission and reception in synchronization with a clock signal (lines 19-23 of page 2), said data processing device comprising:

a central processing unit ("microcomputer" must have a CPU); a clock pulse generation circuit (phi-s in Fig 7 must be generated by a clock pulse generation circuit) for generating a plurality of clock signals (system clock phi-s comprises plurality of clock signal); an interface unit (200) for data transmission and reception to and from the external device (Fig 7), wherein said interface unit includes:

a first external terminal for outputting said clock signal (241);

an output driver (252) for driving said first external terminal based on the clock signal

generated by said clock pulse generation circuit (CLK is based on phi-s) to output the

clock signal (Fig 7); an equivalent load circuit (G3) to generate a clock signal (CLK') for

latching data inputted from said external device (242-254-255 of Fig 7).

The AAPA does not teach the following limitations:

an equivalent load circuit capable of imparting, to the clock signal extracted from an

arbitrary position in a stage previous to output driver in a clock signal path, delay

equivalent to delay resulting from an external load coupled to external terminal in-order

to generate a clock signal for latching data inputted from said external device.

Schaefer teaches the following limitations:

an equivalent load circuit (210) capable of imparting, to the clock signal (202) extracted

from an arbitrary position in a stage previous (CLKD) to output driver (combination of

212a-i and 213a-i are DQ buffers, which are output drivers) in a clock signal path (CLKD

is on the clock signal path) , delay equivalent to delay resulting from an external load

coupled to external terminal (The output driver or buffers are connected to external load.

The output buffer must consider the loading condition, which includes the delay

associated with the load. Thus, delay B must incorporate the delay of load. A supporting

statement can be found in lines 6-15 of [0005] of page 1, which mention that clock can

be offset with delay compensation circuit for variations such as loading conditions.

Thus, the loading conditions are communicated to the delay model 210)

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of AAPA and Schaefer. One ordinary skill in the art would have been motivated to have an equivalent circuit with variable load delay, since that places the data valid window with greater precision (line 15 of [0005] of page 1).

For claim 5, AAPA teaches plurality of second external terminals for receiving data from memory. 242 must comprise plurality of terminals as "CMD" and "DATA" are being inputted. 255 should comprise plurality of latches as plurality of input "DATA", "CMD" are being inputted. The data is latched based on equivalent load circuit G3.

For claim 6, neither AAPA nor Schaefer teaches operating certain part of the circuit with one voltage and operating another part with second voltage. Examiner takes an official notice that operating one part of the circuit with one voltage that is different from another voltage operating on another part is well known in the art. One ordinary skill in the art would be motivated to have two operating voltages in different area of the same circuit to save power consumption.

For claims 9 and 10, 208 of Schaefer comprises a selector circuit to select the appropriate delay and selectively passing the signal through the appropriate delay components. 206 and 208 must store the value necessary to determine the number of

delay elements that needed to be activated. Thus, the circuit comprises a register to store the value for the selector and a decoder necessary to generate the control signals for the selector to select the appropriate number of delay components.

For claim 11, AAPA teaches the non-volatile memory device performing data transmission and reception based on a clock signal outputted from data processing device.

Claims 2, 3, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, in view of Schaefer (US Patent Application Publication 2005/0243635), further in view of Grossnickle et al (US Patent Application Publication 2004/0064749).

For claims 2, 3, 7 and 8, AAPA modified by Schaefer does not teach that the equivalent load circuit is a time constant circuit comprising resistors and capacitors.

Grossnickle et al teach the delay circuit comprising resistors (P1301) and capacitors (CAP0-CAP3). Fig 3 shows the delay circuit comprising time constant circuits for generating signals with different amounts of delay.

It would have been obvious for an ordinary skill in the art at the time the invention was made to combine the teachings of AAPA, Schaefer and Grossnickle. One ordinary skill

in the art would be motivated to have the time constant circuits as taught by Grossnickle

in the system of AAPA as modified by Schaefer to tune the delay settings.

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Fahmida Rahman whose telephone number is 571-272-

8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Lynne Browne can be reached on 571-272-3670. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business

Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO

Customer Service Representative or access to the automated information system, call

800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Fahmida Rahman
Examiner
Art Unit 2116

LYNNE H. BROWNE
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TECHNOLOGY CENTER 2100